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1 Reducing TLB power requirements

Toni Juan, Tomas Lang, Juan J. Navarro

August 1997 **Proceedings of the 1997 international symposium on Low power electronics and design**

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2 Reducing power in superscalar processor caches using subbanking, multiple line buffers and bit-line segmentation

Kanad Ghose, Milind B. Kamble

August 1999 **Proceedings of the 1999 international symposium on Low power electronics and design**

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Keywords: low power caches, power estimation

3 Selective cache ways: on-demand cache resource allocation

David H. Albonesi

November 1999 **Proceedings of the 32nd annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.09 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Increasing levels of microprocessor power dissipation call for new approaches at the architectural level that save energy by better matching of on-chip resources to application requirements. Selective cache ways provides the ability to disable a subset of the ways in a set associative cache during periods of modest cache activity, while the full cache may remain operational for more cache-intensive periods. Because this approach leverages the subarray partitioning that is already pr ...

4 The energy efficiency of IRAM architectures

Richard Fromm, Stylianos Perissakis, Neal Cardwell, Christoforos Kozyrakis, Bruce McGaughy, David Patterson, Tom Anderson, Katherine Yelick

May 1997 **ACM SIGARCH Computer Architecture News , Proceedings of the 24th annual international symposium on Computer architecture**, Volume 25 Issue 2

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